

Appl. No. 10/743,985
Amdt. dated 02/01/2006
Response to Office Action of 11/01/2005

Attorney Docket No.: N1085-00168
[TSMC2003-0219]

Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

1 1 - 10. (Cancelled)

1 11. (Currently Amended): An SOI device having a gate, comprising:
2 oxygen ~~or halogen~~ ions providing implants in a substrate of an SOI device; and
3 one or more additional gate regions covering all implants under the one or more
4 additional gate regions, the ions forming thicker gate oxide regions, and reducing
5 substrate resistance under each of the additional gate regions.

1 12. (Original): The SOI device as recited in claim 11, further comprising:
2 implanted ions in the substrate, the one or more additional gate regions covering
3 the implanted ions.

1 13. (Original): The SOI device as recited in claim 11, further comprising:
2 a gate oxide covering the ions and being under the one or more additional gate
3 regions.

1 14. (Original): The SOI device as recited in claim 11, further comprising:
2 a gate of the SOI device;
3 a gate oxide under the gate and under the one or more additional gate regions;
4 and
5 the gate oxide covering the ions.

1 15. (Original): The SOI device as recited in claim 11, further comprising:
2 a gate electrode layer forming an SOI device gate and the one or more additional
3 gate regions; and
4 a gate oxide layer under the gate and under the one or more additional gate
5 regions.

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1 16. (Original): The SOI device as recited in claim 11, further comprising:
2 an SOI device gate and the one or more additional gate regions being formed
3 from a gate electrode layer; and
4 a gate oxide layer wherein the gate oxide layer is under the gate and under the
5 one or more additional gate regions.

1 17. (Original): The SOI device as recited in claim 11, further comprising:
2 a thin gate oxide layer having a thicker gate oxide covering the ions;
3 an SOI device gate on the thin gate oxide layer; and
4 the one or more additional gate regions being on the thicker gate oxide.

1 18. (Original): The SOI device as recited in claim 11, further comprising:
2 the thicker gate oxide being a selective epitaxy growth.

1 19. (Original): The SOI device as recited in claim 11, further comprising:
2 the substrate having an STI enclosure for the ions.

1 20. (Withdrawn): An SOI device in a substrate on a semiconductor wafer,
2 comprising:
3 a semiconductor layer as part of the substrate;
4 an additional gate electrode on the substrate; and
5 oxygen ions in the substrate forming implants in a gate oxide region under the
6 additional gate electrode.

1 21. (Withdrawn): The SOI device of claim 20, further comprising:
2 doped ion implants under the gate electrode, the doped ion implants forming a
3 source and drain in the substrate.

1 22. (Withdrawn): The SOI device of claim 20, further comprising:

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2 a buried oxide layer covering the semiconductor wafer; and
3 the semiconductor layer being on the buried oxide layer.

1 23. (Withdrawn): The SOI device of claim 20 wherein, the semiconductor layer is a
2 P-substrate, and the doped ion implants are N+ doped ions.

1 24. (Withdrawn): The SOI device of claim 20 wherein, the semiconductor layer is an
2 N-substrate; and the doped ion implants are P+ doped ions.

1 25. (Withdrawn): The SOI device of claim 20, further comprising:
2 at least one additional gate region on the gate electrode; and
3 the oxygen ions forming a thick gate oxide region under said additional gate
4 region.

1 26. (Withdrawn): The SOI device of claim 20, further comprising:
2 additional gate regions on the gate electrode forming an H-gate; and
3 the oxygen ions forming shallow trench isolation regions.

1 27. (Withdrawn): An SOI device in a substrate on a semiconductor wafer,
2 comprising:
3 a semiconductor layer as part of the substrate;
4 a gate electrode on the substrate; and
5 halogen ions in the substrate forming implants in a gate oxide region under the
6 gate electrode.

1 28. (Withdrawn): The SOI device of claim 27, further comprising:
2 doped ion implants under the gate electrode, the doped ion implants forming a
3 source and drain in the substrate;

1 29. (Withdrawn): The SOI device of claim 27, further comprising:

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2 a buried oxide layer covering the semiconductor wafer; and
3 the semiconductor layer being on the buried oxide layer.

1 30. (Withdrawn): The SOI device of claim 27 wherein, the semiconductor layer is a
2 P-substrate, and the doped ion implants are N+ doped ions.

1 31. (Withdrawn): The SOI device of claim 27 wherein, the semiconductor layer is an
2 N-substrate, and the doped ion implants are P+ doped ions.

1 32. (Withdrawn): The SOI device of claim 27, further comprising:
2 at least one additional gate region on the gate electrode; and
3 the halogen ions forming a thick gate oxide region under said additional gate
4 region.

1 33. (Withdrawn): The SOI device of claim 27, further comprising:
2 additional gate regions on the gate electrode forming an H-gate; and
3 the halogen ions forming shallow trench isolation regions.

1 34. (Withdrawn): The SOI device of claim 27 wherein, the halogen ions are fluorine
2 ions.

1 35. (New) An SOI device having a gate, comprising:
2 fluorine ions providing implants in a substrate of an SOI device; and
3 one or more additional gate regions covering all implants under the one or more
4 additional gate regions, the ions forming thicker gate oxide regions, and reducing
5 substrate resistance under each of the additional gate regions